Reduction of Tombstone Capacitor Problem by Six Sigma Technique: A Case Study of Printed Circuit Cable Assembly Line

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Abstract – **This paper demonstrated the implementation of Six Sigma technique and DMAIC improvement methodology into a mass manufacturing of printed circuit cables. The result showed that by following the theoretical Six Sigma technique and DMAIC steps, the defects from major tombstone capacitor problem could be reduced from 1,154 DPPM to 314 DPPM and increased 1st yield output from 98.4% to 99.66%.**

Keywords – **Printed circuit cable assembly, Six Sigma, DMAIC, Tombstone capacitor problem**

I. INTRODUCTION

Six Sigma has become a successful quality level improvement methodology since 1980s. This technique has been deployed in a large number of leading industries since 1990s for production cost saving [1], net profits and operating margin improvement worldwide [2-4].

The company in this case study is one of leading electronic manufacturing service companies such as arm, coil, e-box, and panel for hard disk drive assembly. The company has faced tombstone component problems (as shown in Fig. 1) especially the capacitor component in the printed circuit cable assembly process up to 48% of all problems occurred which led to 613 defects part per week or 1,154 DPPM (defect part per million). The problem led to the 1st yield output rate to only 98.4% and affected manufacturing and quality costs. The objective of this study focused on reducing tombstone capacitor problem to at least 70% by implementing the Six Sigma technique and its DMAIC improvement methodology.

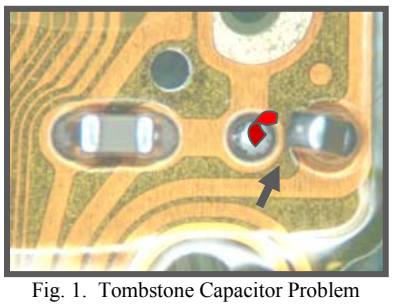

Fig. 1. Tombstone Capacitor Problem

II. METHODOLOGY

Brue [5] has stated that Six Sigma is a revolutionary business process for reducing organizational inefficiencies as well as a business performance improvement strategy that aims to reduce the number of defects to 3.4 defect parts per million opportunities [6]. This Six Sigma method originated at Motorola Company aimed to improve product quality in the 1980s according to process variation concept of Professor Edward W. Deming; father of Quality Improvement [7].

Does [8] has expressed 3 meanings of Six Sigma as following:

1) A business strategy for competitive advantage
2) A philosophy to work smarter by decreasing mistakes, indicating sources of variation and improving process capability.
3) A statistical measurement tool to display the quality of product/service and its transformation processes.

The Six Sigma methodology starts and ends with customer satisfaction. Therefore, it should be spreading throughout the company, with continuous employee training to have strong foundation process improvement team [9-11].

With the evidence of the Six Sigma program benefits, its methodology has been adopted worldwide in both manufacturing and service industries. The early adopters of Six Sigma are electronic and computer and communication (C&C) industries [12].

In Thailand, various industries applied the Six Sigma for defect reduction purposes; for example, an automotive industry [13,14], an electronic industry [15,16], a plastic industry and a metallurgical industry [17,18]. Their applications of Six Sigma used a number of tools including seven basic quality control tools (7QC tools), a process mapping, a failure mode and effect analysis (FMEA), an analysis of variance (ANOVA) and a design of experiment (DOE), and a measurement system analysis (MSA). This study also applied these tools according to DMAIC steps as shown in Fig. 2 and Fig. 3.

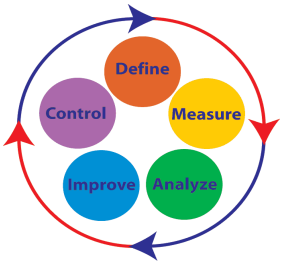

Fig. 2. DMAIC Continuous Improvement Process

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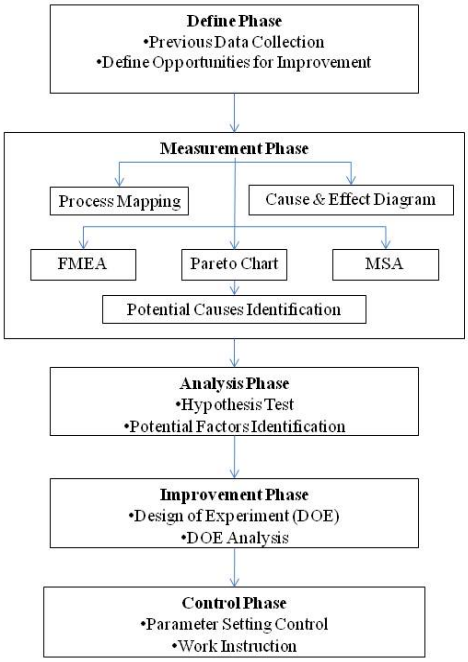

Fig. 3. Methodology

The Six Sigma requires a team effort. For this study, a team of 6 persons was gathered comprising of a process engineer, a process engineering manager, a process supervisor, a maintenance engineer, a process quality control engineer and a process control technician. With brainstorming, each of DMAIC steps requires these following considerations:

1) *Define Phase*: the define phase aimed to prioritize opportunities for improvement by quantifying any known or perceived opportunities. The problem was stated in term of how much, when, where and how. The impacts of customer reliability and product quality as well as potential cost savings were identified.
2) *Measurement Phase*: this phase intended to measure all failures. In order to search for root causes, a number of basic and advanced statistical tools were applied. A process mapping could point out possibilities of which process might cause the problem and which process could detect the problem. The cause and effect (C&E) diagram illustrated all known input and output relationships. The failure mode and effect analysis (FMEA) and the Pareto chart of risk priority numbers (RPN) were used for searching the most possible causes of the problem. The Measurement System Analysis (MSA) was applied to improve operator and automatic optical inspection machine measurement efficiencies.
3) *Analysis Phase*: A 2 proportion one-way ANOVA was used to screen all possible causes. The statistically significant ones were targeted for the improvement phase.
4) *Improvement Phase*: the factorial Design of Experiment (DOE) was suitable for studying main effects and interactions between factors. The result from DOE would show the most appropriate setting of key factor input values (KPIVs) that give the optimum key factor output value (KPOV).
5) *Control Phase*: the control phase focused on monitoring, checking, and assessing the process until the defects were reduced to meet target with applications of the statistical process control (SPC) and internal audit.

III. RESULTS

A. Define Phase

Printed circuit cable assembly line for this study has a maximum capacity of 2.01 million units per week. Top 5 problems occurred in the assembly lines included 1) tombstone capacitor, 2) solder pad capacitor exposure, 3) misaligned connector, 4) tombstone resistor and 5) under-filled expose as shown in Fig. 4. Tombstone capacitor ranked number 1 which was considered a major problem accounted for 48% or 1,154 DPPM. Thus, the improvement team has defined tombstone capacitor problem as an opportunity for improvement.

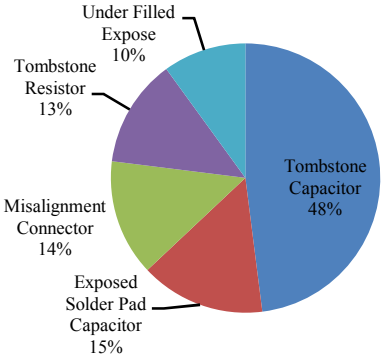

Fig. 4. Printed Circuit Assembly Problem Identification

B. Measurement Phase

The process mapping diagram as shown in Fig. 5 indicated that the tombstone capacitor problem occurred at process number 2 (solder paste printing process), process number 3 (component placement process) and process number 5 (reflow soldering process). The tombstone capacitor problem could be 100% detected at a process number 8 (Automatic Optical Inspection, AOI) by using an automatic optical machine.

The cause and effect diagram in Fig. 6 showed all possible causes to the tombstone capacitor problems categorized into man, machine, materials, method, measurement and environment factors.

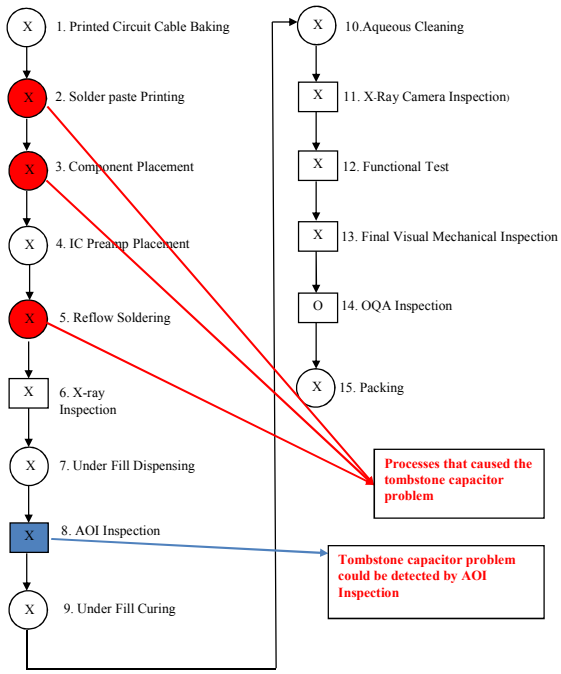

Fig. 5. Printed Circuit Cable Assembly Process

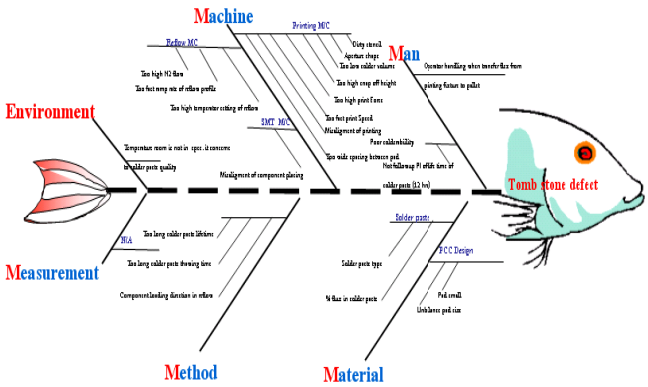

Fig. 6. Cause and Effect Diagram

The FMEA analyzed all 21 causes listed in the C&E diagram. The risk priority numbers (RPN) were calculated as listed in Table I. The Pareto chart was plotted to list the RPNs from the highest to the lowest as shown in Fig. 7. Six potential causes with RPN score higher than 100 were selected for further analysis in the next phase.

TABLE I
RPN SCORE OF ALL POTENTIAL CAUSES OF FAILURE

Category	No.	Potential Causes of Failure	RPN
Man	1	Handling flex from printing fixture to pallet	32
Machine	2	Too low solder volume	384
	3	Dirty stencil	32
	4	too high snap of height	32
	5	Too fast printing speed	32
	6	Too high printing force	32
	7	Misalignment of printing	16
	8	Aperture shape	144
	9	Too wide pad spacing	288
	10	Misalignment of component placing	192
	11	Too high N_2 flow rate	224
	12	Too fast ramp rate of reflow profile	192
	13	Too high temperature setting of reflow	32
Materials	14	% flux in solder paste	16
	15	Solder paste type	16
	16	Too small pad	48
	17	Unbalance pad size	48
Method	18	Component loading direction in reflow	32
	19	Too long solder paste thawing time	96
	20	Too long solder paste life time	96
Environment	21	Room temperature is out of control	32

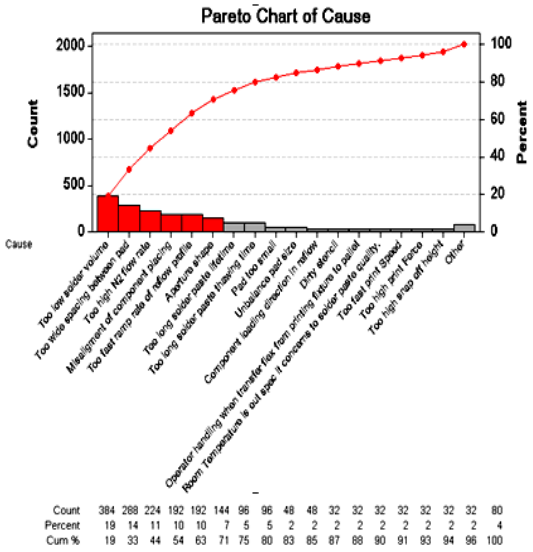

Fig. 7. Pareto Chart of Potential Causes

The MSA was applied to improve the operator and automatic optical inspection machine measurement efficiencies. For AOI machine, an attribute gage R&R report showed a 100% consistency and 100% efficiency in detecting accepted and rejected parts. For operators who perform a solder paste height measurement, the % contribution showed satisfactory repeatability and reproducibility.

C. *Analysis Phase*

The one-way ANOVA was used to check all 6 potential factors and found that only 3 factors were statistically significant as shown in Table III.

TABLE II
STATISTICALLY SIGNIFICANT FACTORS

No.	Factor	RPN	Hypothesis Test
1	Too low solder volume	384	Significant
2	Too wide pad spacing	288	Significant
3	Too high N_2 flow rate	224	Insignificant
4	Misalignment of component placing	192	Insignificant
5	Too fast ramp rate of reflow profile	192	Significant
6	Aperture shape	144	Insignificant

D. Improvement Phase

The team brainstormed and selected factors and levels to conduct a 2^3 full factorial experimental design as shown in Table IV.

TABLE IV
FACTORS AND LEVELS IN 2^3 FULL FACTORAIAL DESIGN

Factor	KPIV		Unit
	Current	Proposed	
Solder volume	5	6.5	mil
Pad spacing	13	9	mm
Reflow profile	Ramp	Soaking	

Main effects plot in Fig. 8 demonstrated that the tombstone defective rate decreased when solder volume (factor A) reduced from 5 mils to 6.5 mils, when pad spacing (factor B) reduced from 13 mm. to 9 mm. and when changing reflow profile (factor C) from Ramp to Soak. Fig. 9 showed interactions plot among factors. There were no interactions between solder volume and pad spacing (AB interaction), solder volume and reflow profile (AC interaction) and pad spacing and reflow profile (BC interaction)

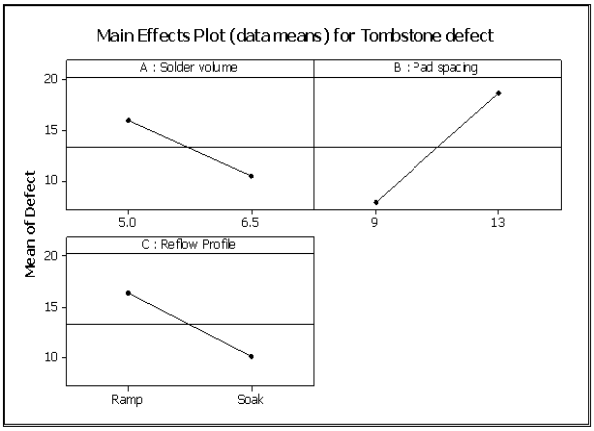

Fig. 8. Main Effects Plots

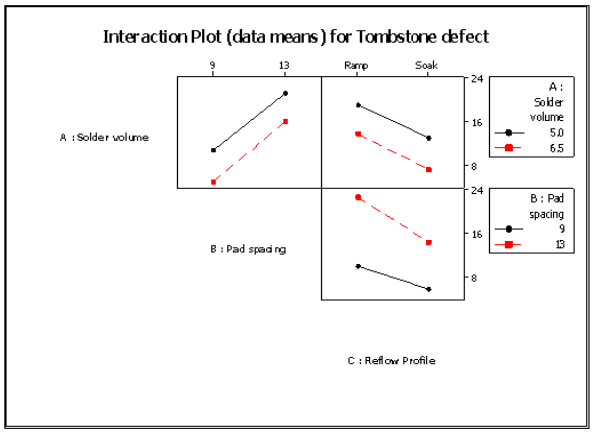

Fig. 9. Interaction Plots

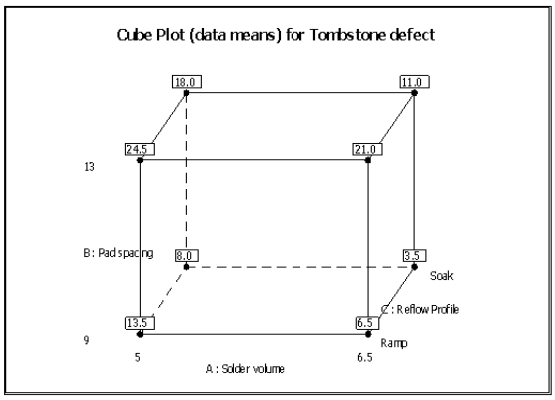

Fig. 10. Factorial Cube Plots

Fig. 10 showed factorial design cube plot which demonstrated opportunities of improvement by controlling the factor setting at solder volume of 6.5 mil, pad spacing at 9 mm. and soaking reflow profile. It yielded an optimum setting to solve the tombstone capacitor problem.

E. Control Phase

The solder volume and reflow profile factors could be controlled by the parameter setting control while the pad spacing factor was controlled through stencil drawing design. After implementing the suggested factor setting, there was a remarkable reduction of the tombstone capacitor problems as shown in Fig. 11. The average defective rate was reduced from 1,154 DPPM to 903 DPPM and finally at 314 DPPM. Mean and range control charts were implemented to assure that the process was under control.

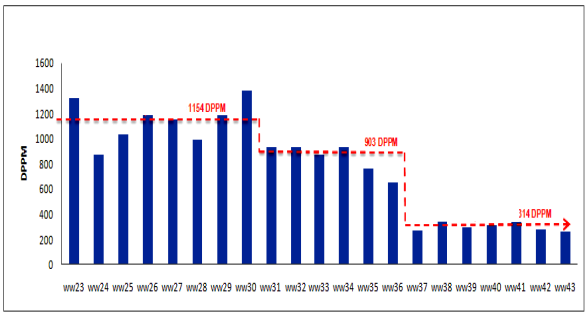

Fig. 11. Defective Average After Improvement

IV. DISCUSSION AND CONCLUSION

This project has demonstrated the power of the Six Sigma technique and its DMAIC methodology to solve the tombstone capacitor problem in the Printed Circuit Cable Assembly line.

The problem was defined, measured, analyzed with the solution ready to implement in a short period of time. The self-direct team with involving employees has

generated ideas to solve the problem. The implementation of tools associated with Six Sigma DMAIC process allowed this project to solve the tombstone capacitor problem with the outcome of defect reduction from 1,554 DPPM to 314 DPPM which accounted for 73% with higher acceptable output (yield) at 99.66% as shown in Fig 12.

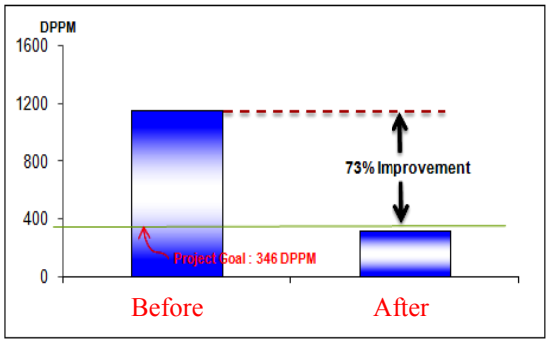

Fig. 12. Before and After Defective Average

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